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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/574,290	03/31/2006	Mitsuaki Osame	0756-7670	7471

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Robinson Intellectual Property Law Office, P.C.
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EXAMINER	
NGUYEN, LONG T	

ART UNIT	PAPER NUMBER
2816	

MAIL DATE	DELIVERY MODE
04/14/2011	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/574,290	OSAME ET AL.	
	Examiner	Art Unit	
	LONG NGUYEN	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 March 2011*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *22-25 and 29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *22-25 and 29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 April 2009* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/23/11*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under Ex Parte Quayle, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 3/23/11 has been entered.

2. In this office action, the indicated allowability of claims 22-25 and 29 are withdrawn in view of the newly discovered reference(s). Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 22 and 25 are rejected under 35 U.S.C. 102(b) as being anticipated by Tomisawa (USP 5,039,893).

For claims 22 and 25, Figure 9 of Tomisawa teaches a semiconductor device including: a first transistor (PMOS 16), a second transistor (NMOS 18), a plurality of inverters (10-1, 10-2, 10-3, ... 10-n), a first power source for applying a first potential (Vdd), a second power source for applying a second potential (Vss), a first circuit (circuitry generates v2) for generating a third

potential (v2) different from the first and second potentials, a second circuit (circuitry generates v1) for generating a fourth potential (v1) different from the first and second potentials; wherein each inverters includes: a third transistor (PMOS 12) and a fourth transistor (NMOS 14), wherein one of a second and drain of the second transistor (NMOS 18) is connected to the second power source (Vss), wherein the other one of the source and drain of the second transistor is connected to each of the plurality of inverters (10-1, 10-2, 10-3, ... 10-n); wherein one of the source and drain of the first transistor (PMOS 16) is connected to the first power source (Vdd), wherein the other of the source and drain of the first transistor is connected to each of the plurality of inverters (10-1, 10-2, 10-3, ... 10-n); wherein the first transistor (PMOS 16) and the second transistor (NMOS 18) are connected to each other with at least one of the plurality of inverters (10-1, 10-2, 10-3, ... 10-n) interposed therebetween, wherein a gate of the first transistor (PMOS 16) is connected to the second circuit (circuitry generates v1), a gate of the second transistor (NMOS 18) is connected to the first circuit (circuitry generates v2), wherein a first signal is inputted to gates of the third transistor and the fourth transistor of each of the plurality of inverters (gates of transistors in first inverter 10-1 receive input 13, gates of transistors in second inverter 10-2 receive an input from the output of inverter 10-1, gates of transistors in third inverter 10-3 receive an input from the output of inverter 10-2, etc.), wherein a second signal is outputted from one of a second and a drain of the first transistor and one of a source and a drain of the fourth transistor of each of the plurality of the inverters (each inverters 10-1, 10-2, 10-3 ... 10-n generates an output at the junction source/drain connections of the PMOS and NMOS transistors in that inverter, see Figure 9).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tomisawa (USP 5,039,893) in view of Uchiki et al. (USP 6,646,486).

With respect to claims 23 and 24, Figure 9 of Tomisawa teaches all the limitations of these claims as discussed in the 102 rejection above except for each of the first and second circuits includes multiples resistors connected in series between the first power source and the second power source, wherein the third (or fourth) potential is outputted from a connecting node of two resistors that are selected from the multiple resistors. However, Figure 12C of the Uchiki et al. teaches a voltage divider generator circuit that includes a plurality of resistors (R1, R2) connected in series between the first power source (Vdd) and the second power source (GND), wherein the third/fourth potential (N1) is outputted from a connecting node (N1) of two resistors (R1, R2) that are selected from the multiple resistors. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the circuitry in Figure 9 of Tomisawa by specifically using the voltage divider generator of Figure 12C for each of the first and second circuits to generate the third and fourth potentials (v2 and v1), respectively, for the purpose of easily achieving a known reference voltage based on the ratio of the fixed resistances of the resistors. Thus, this modification/combination meets all the limitations of claims 23 and 24.

7. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tomisawa (USP 5,039,893).

With respect to claim 29, Figure 9 of Tomisawa teaches all the limitations of this claim except that the third potential is different from the fourth potential. However, Tomisawa also teaches that the values of voltages v1 and v2 are set at values which are symmetrical to the references voltages (Vdd - Vss) to control the delay of the circuitry, so it is seen that the specific values of v1 and v2 are set based on the design choice, i.e., depending on the need of the circuit designer to have a specific delay in the circuitry for a certain application. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the cirucitry of Figure 9 of Tomisawa by specifically using the third potential (v2) different from the fourth potential (v1) for the purpose of achieving a certain delay time of the circuitry depending on the need of the designer for a specific application.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Thursday from 8:00am to 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lincoln Donovan, can be reached at (571) 272-1988. The fax number for this group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Long Nguyen/
Primary Examiner
Art Unit 2816